Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **NC**
2. **CAP +**
3. **GND**
4. **CAP –**
5. **VOUT**
6. **LV**
7. **OSC**
8. **V +**

**.073”**

**5**

**6**

**7**

**8 1**

**4**

**3**

**2**

**MASK**

**REF**

**7660**

**.069”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 7660**

**APPROVED BY: DK DIE SIZE .069” X .073” DATE: 7/25/23**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: SIS7660**

**DG 10.1.2**

#### Rev B, 7/1